Steven Mu

smu@uwaterloo.ca LinkedIn Profile GitHub Page Project Portfolio

Skills

Languages & Build Systems: C (User and Kernel space), C++, ARMv8 ISA, RISC-V ISA, System Verilog, Verilog, Python, Bash, Make, Meson
Tools & Environments: UNIX CLI, Linux, Embedded Linux, FreeRTOS, GDB, GCC, Git, Docker, Protocol Buffers, SQLite, GTest
Standards & Protocols: Scrum/Agile (Jira & Confluence), MISRA C, Gitlab & Jenkins CI/CD, JTAG Debuggers, CAN, UART, I2C, (Q)SPI
Other Skills: Altium, AMD Vivado, PCB Fab, Circuits, Datasheets, Oscilloscopes, OnShape, Wireshark

Professional Experience

System Software Engineering Intern – **Tesla**

Austin, TX, United States Jan 2026 - Apr 2026

- Current intern on Infotainment System Software team. Working in **C / C++** on display firmware & network performance monitoring

Embedded Software Engineering Intern – **Kepler Communications**

Toronto, ON, Canada May 2025 - Aug 2025

- Flight Software team, developed embedded solutions for a satellite fleet to bring high-speed connectivity to space (Launch Jan 2026)
- Worked with **C and C++** on a very resource-constrained and timing-critical **AMD Zynq** SoC (**ARM Cortext-A53**, **Cortex-R5F, FPGA**)
- Led design & development of a **C++** embedded config manager w/ **Protobuf** & **SQLIte3**. Added 95%+ coverage tests w/ **Google Test**
- Developed an embedded publish-subscribe message framework w/ **ZeroMQ**. Using that, built a service API used across 10 satellites
- Assisted integration of a flight software **build system** using **Meson**. Optimized **Embedded Linux** (Petalinux) build system w/ **bitbake**

Firmware Engineering Intern – **Ford Motor Company**

Ottawa, ON, Canada Sep 2024 - Dec 2024

- Bootloader, BSP & Kernel team, developed drivers with **C in User & Kernel space** for **ARM Cortex-A53** SoC w/ resource-constraints
- Improved bootloader stability, reducing boot fails caused by **LPDDR Memory, eMMC and Interrupt Controller (GIC-500)** to < **0.001%**
- Improved **Embedded Linux Kernel** by optimizing peripherals during suspend & resume. Also added callstack dumps in kernel panic
- Worked with debug hardware (Lauterbach PowerDebug **JTAG + TRACE32**) for memory level debugging. Managed work w/ Atlassian

Embedded Software Intern – **450 Solutions**

Tokyo, Japan (Remote) Jan 2024 - Apr 2024

- Power & Performance Firmware team, contributed to high level design, as well as driver development for a Point-of-Sale system.
- Worked with **C and C++** to develop drivers for a **Bluetooth LE** printer system. Also worked on optimizing power usage by interfacing with **display drivers** and the onboard **PMIC**. Improved end-to-end printing speed by **25%** and reduced display power usage by **15%**

Interfacing Team Co-Lead – **WATONOMOUS**

Waterloo, ON, Canada Jan 2024 - Aug 2024

- Co-led the development of vehicle systems. Developed sensor software in **C** to collect & send metrics to a Centralized Info System
- Worked with **Altium** to design & fabricate PCBs, including the distance sensor **controller** and its **Power** & **Communication** boards

Personal Projects

Bare-Metal Bootloader & RTOS (SprinterOS) (Click to Learn More)

Dec 2024 - Present

- Hobby **bare-metal** board bringup (bootloader & kernel) for an **ARM Cortex-M7** based STM32F767ZI, without HAL or any libraries
- Bootloader and Kernel done using **C** and **ARMv7 Assembly,** with custom graphics driver & accelerator done in **Verilog**
- **Boot & Bringup**: Clock, UART, GPIO, Watchdog Timer, External SD Flash driven by SPI, Boot-to-Kernel Transition, Boot Power Modes
- **Kernel & BSP**: Pre-emptive Scheduling, Context Switching, Dynamic Mem Allocation, Mem Protection, Power Modes, Interrupts, IPC
- Used debug hardware (**SEGGER J-Link JTAG & STLink**) and **GDB** to perform memory and register level debugging & verification
- Working on an FPGA based graphics unit w/ a Xilinx Spartan-7 XC7S50 board, using **Verilog** in **Vivado**. Interfaced w/ STM using **QSPI**

RISC-V 5-Stage Pipelined Datapath (Click to Learn More)

Sep 2025 – Dec 2025

- Designed and implemented a 5-stage, in-order, pipelined RISC-V datapath in **Verilog**. Simulated in **xsim** and testing on a **PYNQ FPGA**
- Added data forwarding, and hazard detection. Also designed a BRAM Register File & Data/Instruction Memory. Wrote testbenches

Education

University of Waterloo

Waterloo, ON, Canada

BASc - Computer Engineering Senior, Expected Grad: Apr 2027

- UWaterloo Varsity Men's Track and Field, ECE Wellness & Athletics Representative, UW Athletics & Recreation Student Leader
- **Awards:** USPORTS Academic All-Canadian (80%+ avg. as student athlete), B.P Dammizio Scholarship, President's Award of Distinction
- **Relevant Coursework:** Real-Time Operating Systems, Computer Architecture, Compilers, Networks, Digital Hardware (Verilog), Embedded MCU Systems, Control Systems, Data Structures & Algorithms, UNIX System & Concurrency Programming, Circuits, OOP